Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-18 (Canceled).

19 (New): A semiconductor memory device having a memory structure in which a plurality of 5-transistor cells each including first and second CMOS (complementary metal oxide semiconductor) inverter circuits having a latch structure and a control transistor which is connected between a storage node of the first CMOS inverter circuit and a bit line and whose gate is connected to a word line are connected to a plurality of bit lines and a plurality of word lines, the semiconductor memory device comprising:

at least one power line connected to a source terminal of an N-type MOS transistor of at least the second CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines; and

at least one selection circuit which applies second voltage, which is different from a first voltage, to the source terminal of the N-type MOS transistor of the second CMOS inverter circuit of the 5-transistor cells through said at least one power line in a "1" data write mode, or applies the first voltage to the source terminal of the N-type MOS transistor of the second CMOS inverter circuit of the 5-transistor cells through said at least one power line in another mode.

20 (New): The semiconductor memory device according to Claim 19, wherein said at least one power line is connected to a source terminal of an N-type MOS transistor of the first CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines, and said at

least one selection circuit applies the second voltage to the source terminal of N-type MOS transistor of the first and second CMOS inverter circuits of the 5-transistor cells through said at least one power line in the "1" data write mode.

21 (New): The semiconductor memory device according to Claim 19, wherein the second voltage is different from the first voltage by a predetermined voltage.

22 (New): The semiconductor memory device according to Claim 19, wherein the differences between the second voltage and the first voltage is 5% to 30% of the first voltage.